Double-sided probing system for 150µm pitch co-packaged optics

By Collins Sun [WinWay Technology]

The focus of the double-sided probing system described in this article is to be in alignment with trends in networking development. As expected, advanced packaging technology will continue to extend Moore's Law, particularly the rapid development of heterogeneous integration (HI). According to various organizations, such as IEEE, SEMI, and ASME, the essential spirit of HI is to integrate different process nodes and application-specific integrated circuits (ICs) into a single high-end package, such as a 3D structure system-in-package (3D SiP). When HI is combined with silicon photonics (SiPh), trace loss from pluggable optics is greatly reduced and is able to drive higher performance Ethernet applications to 800G (see **Figure 1**).

Individual active and passive optical components in a package can provide the best performance and cost benefits in a comprehensive manner. However, more sophisticated processes in package assembly also mean that it is critical to have the assured yield after assembling all the discrete chips. Co-packaged optics (CPO) is one representative application—its optical signal has a better signal-to-noise ratio than electrical signals because of the light being transmitted through an optic fiber rather than electrical signals through a copper trace. Having optical engines near the electrical switch to reduce signal trace length in the substrate by advanced package technology is a breakthrough technology. According to Yole Intelligence, the compound annual growth rate (CAGR) of the CPO market is predicted at around 55%, from US$6 million in 2020 to US$2.2 billion by 2032 [1].

SiPh have been considered a unique technology for developing high-performance networking system because of several factors. First, it can be designed and manufactured using current complementary metal-oxide semiconductor (CMOS) processes and equipment, thereby achieving lower cost and higher performance devices. Second, it can be combined with logic and digital circuits for data processing. Third, SiPh can be designed using different wafer materials, such as III-V compound semiconductors. The future of SiPh will flow into two main streams: co-packaging and chip integration. Co-packaging is the 2.5D integration of the CMOS logic or digital chip with optical

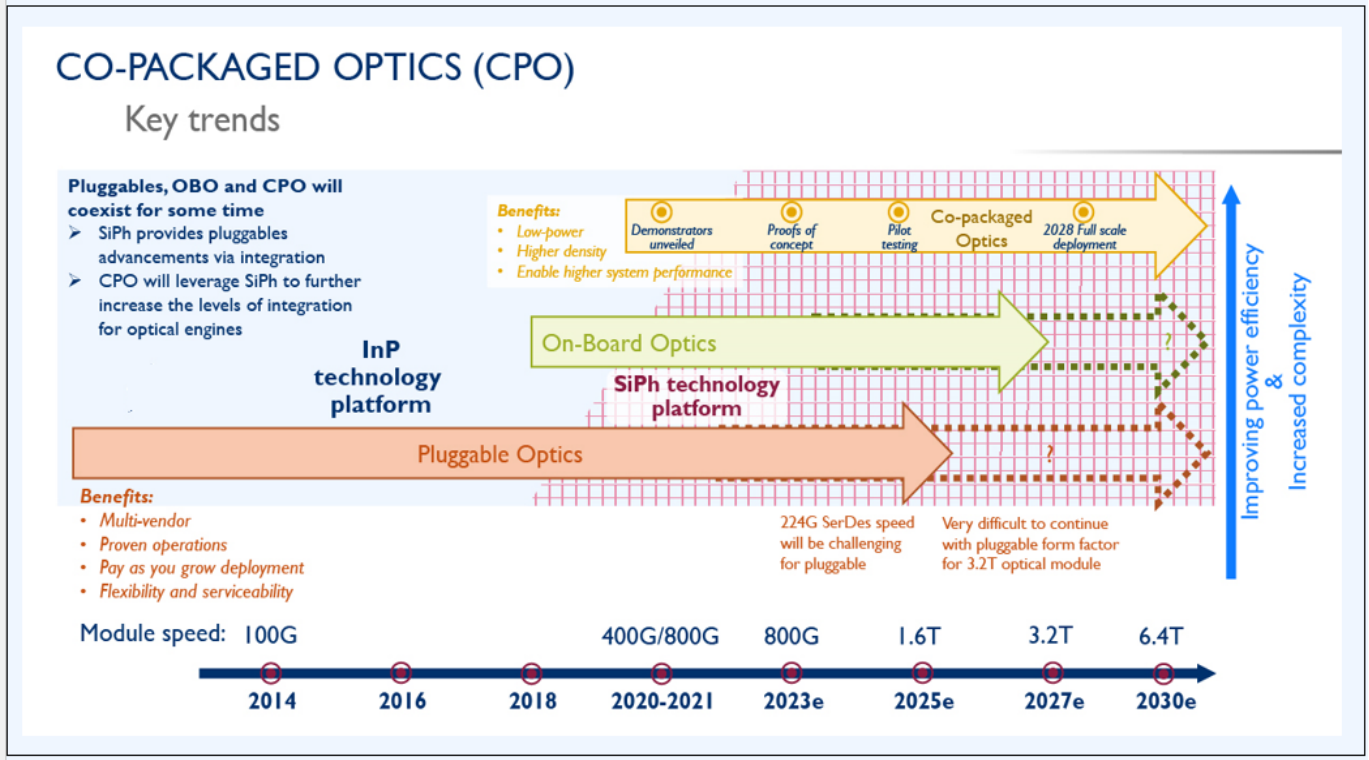

Figure 1: Development trends in pluggable optics and CPO. SOURCE: Yole Group

chips connected by the copper trace of substrate. Chip integration is a single complete chip solution that includes different functional ICs using through-silicon vias (TSVs) both for ASICs and optical die. SiPh are expected to integrate all optical components, such as filter, polarization diversity, and splitter/combiner into a single die, including an active laser, modulator, and photodetector. With the help of SiPh and photonic integrated circuits (PICs), CPO applications will be more competitive overall when compared to conventional pluggable optical modules.

The packaged optical component usually requires a smaller form factor with a fine pitch. Therefore, the testing system needs precision alignment for probing C4 sides approximately 150µm from the top side, and it also must overcome thermal expansion when testing at different temperature points. These are the initial requirements for the double-sided probing system for 150µm-pitch CPO.

Double-sided probing system

The targeted specifications of CPO packaging are listed in **Figure 2**. A double-sided probing system is needed to probe four sites of 150µm-pitch micro-bumps on the top and 1.0mm land grid array (LGA) pad design on the bottom of the package. The major challenges that CPO testing must overcome are: 1) fine pitch, 2) high power, 3) high speed, and 4) a wide temperature range from room temperature (RT) to 105°C. The required test speed is up to 112Gbps, and the dissipation power of the switch application-specific integrated circuit (ASIC) chip is 600W, which needs to be tested at 105°C.

As for testing the fine-pitch CPO package, the most critical aspects include: 1) a very different pitch range for the top and bottom sides of the package, which presents serious difficulties in aligning the contact at the same time; 2) picking and placing the package in a double-sided probing design within the precision alignment requirement; 3) controlling thermal expansion at different testing temperature points to reduce the thermal gradient when probing micro-bumps; 4) achieving extremely high-speed 112Gbps test requirements

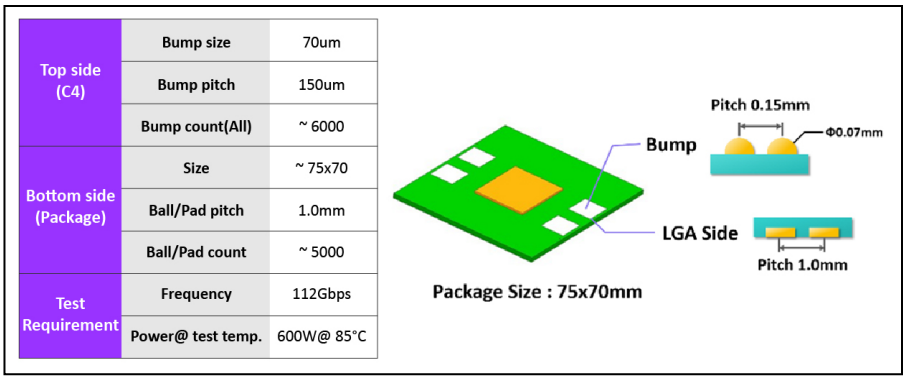

Figure 2: CPO device information.

using a 150µm-pitch wafer-level chip-scale package (WLCSP) probe head—this trend involves testing a wafer-level package at the required speed to distinguish known good dies (KGD); and 5) 600W device power must be dissipated by integrating a 150µm-pitch WLCSP probe head design, in which thermal expansion will lead to unstable contact with the fine-pitch probe.

To summarize from the above challenges: there is a need for a highly-integrated probing system that considers precision alignment and balances thermal and electrical design in a comprehensive thermal chuck design with a 150µm WLCSP probe that provides a stable contact system to handle a 100kg reflected force when testing. To meet these requirements, we propose a test module using an electric loopback interposer and bottom socket, as shown in **Figure 3**.

In the current double-sided probing system, there are four major modules that integrate the whole functionality of CPO testing requirements (**Figure 4**). The four modules are discussed below.

Actuator. The plunger is used in the actuator design to ensure a total 600kg force that can provide a stable contact force to fulfill future trends for large packages. Such packages will need to overcome the total reflected force from the WLCSP probe head and bottom socket. The mechanical strength of the probing system must be considered when applying such high force conditions. It is critical to have a strong structure to reduce micro-vibrations when connecting with the tester and performing thermal control.

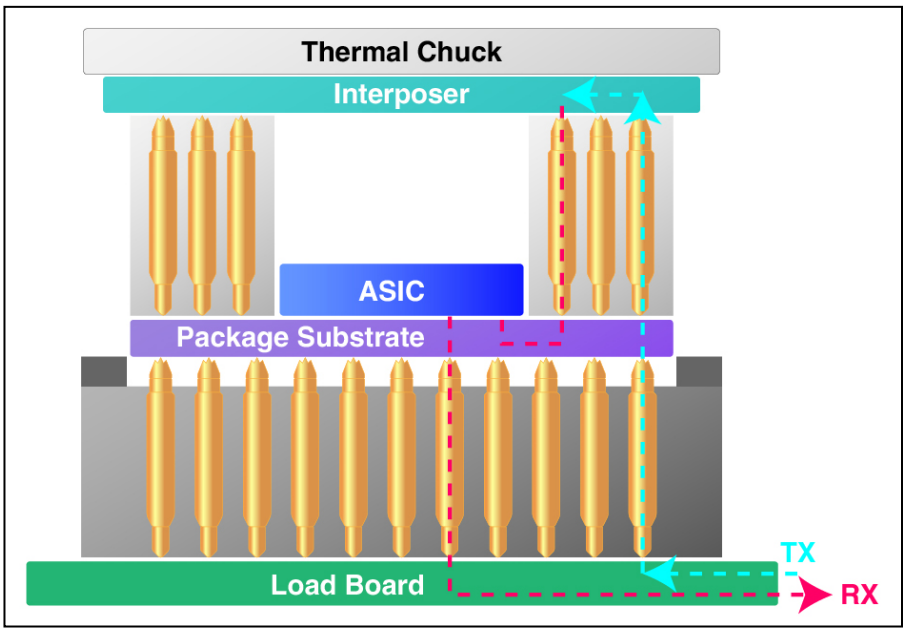

Figure 3: Proposed test module for double-sided probing design.

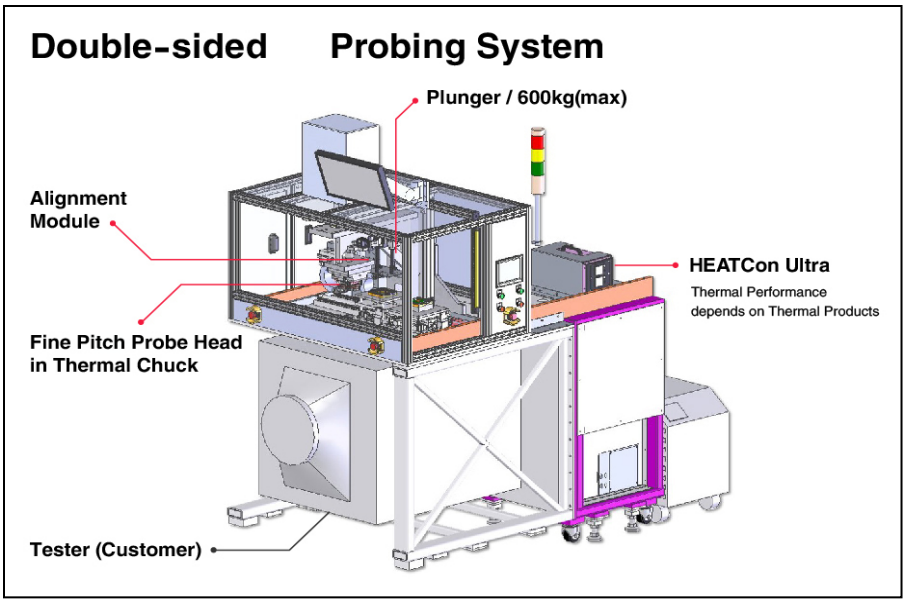

Figure 4: Double-sided probing system.

Alignment. The alignment module is a dual-charge-coupled device (CCD) module combined with a 3-axis X-Y-Θ heating shuttle design to ensure precise alignment when the temperature varies. High-resolution dual-CCD cameras are used to take a picture of the micro-bump on the top side of the package to align every package to the accurate position before picking up the device under test (DUT). Moreover, the heating shuttle plate can reduce the soaking time before reaching thermal equilibrium at the required testing temperature; it also plays an important role in auto calibration before each pick and place action on the package. Because the DUT and probe head are not on the same side, one issue is aligning the tip of the probe head with the micro-bump on the DUT.

We used a dummy device to transfer printing of the probe mark of the probe head tip and perform self-calibration by computing the relative distance to ensure the proper alignment of the probe tips to the device micro-bumps. However, thermal expansion at high temperatures will cause the alignment to be further from the original position by approximately 90µm from what it was at the initial temperature, as shown in **Figure 5**. A multiple stacked structure design that uses different materials causes nonlinear thermal expansion. It has also been proven that the trace of a temperature-dependent probe mark is repeatable. The displacement around 90µm from the initial location at 25ºC to the high temperature of 105ºC is even greater than the diameter of the size of the micro-bump at approximately 70µm, which easily causes contact instability. In consideration of the thermal expansion effect, two separate double-sided probe heads were designed so they could be adjusted to accurate positions by use of fiducial markers and precision guide pins during assembly. However, this design still requires optical re-alignment to check the precision of the final position at each testing temperature point to ensure contact stability and repeatability.

Probe head/thermal control. The high-speed and fine-pitch probe head integrated with a high-performance thermal control system is the most critical design module of the double-sided probing system. To reach the requirement for 112Gbps for the pulse amplitude modulation 4 signal (PAM4), every step in the design of the probe head must be carefully checked by simulation. Channel simulation results, including that for package substrate, fine-pitch probe head, and the loopback interposer, show the behavior of insertion, return loss, and the impedance curve (**Figure 6**).

The targeted impedance value is 93Ω, so closely achieving the values and reducing the impedance mismatch must be considered for each component. Based on the simulation results, the high-speed requirement for 112Gbps PAM4 after integration with whole channel simulation was achieved. Moreover, to prove the simulation result at the boundary condition, we used a simplified test jig in our lab environment with a four-probe double-sided probe station and a 110GHz performance network analyzer (PNA), the results

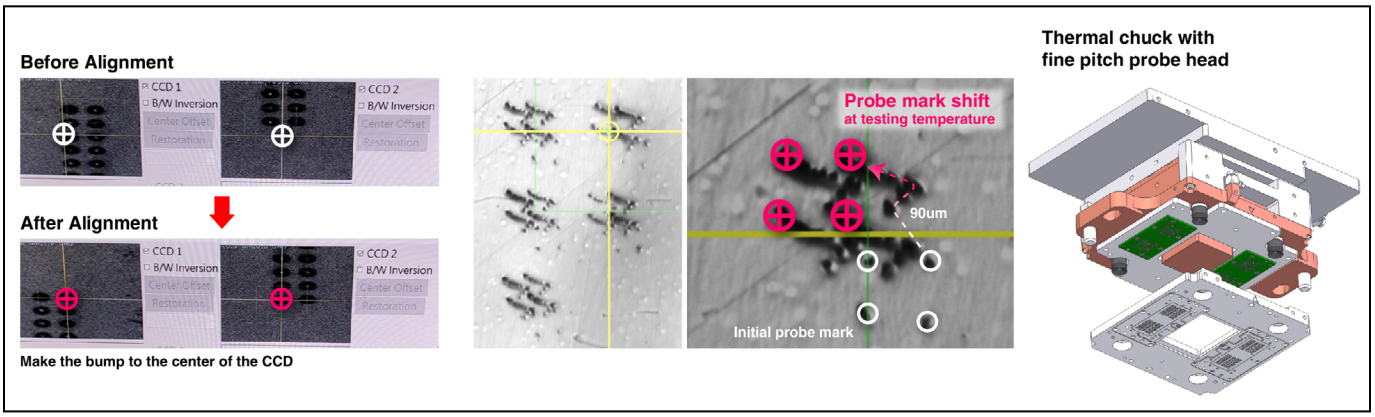

Figure 5: Optical alignment changes with thermal expansion.

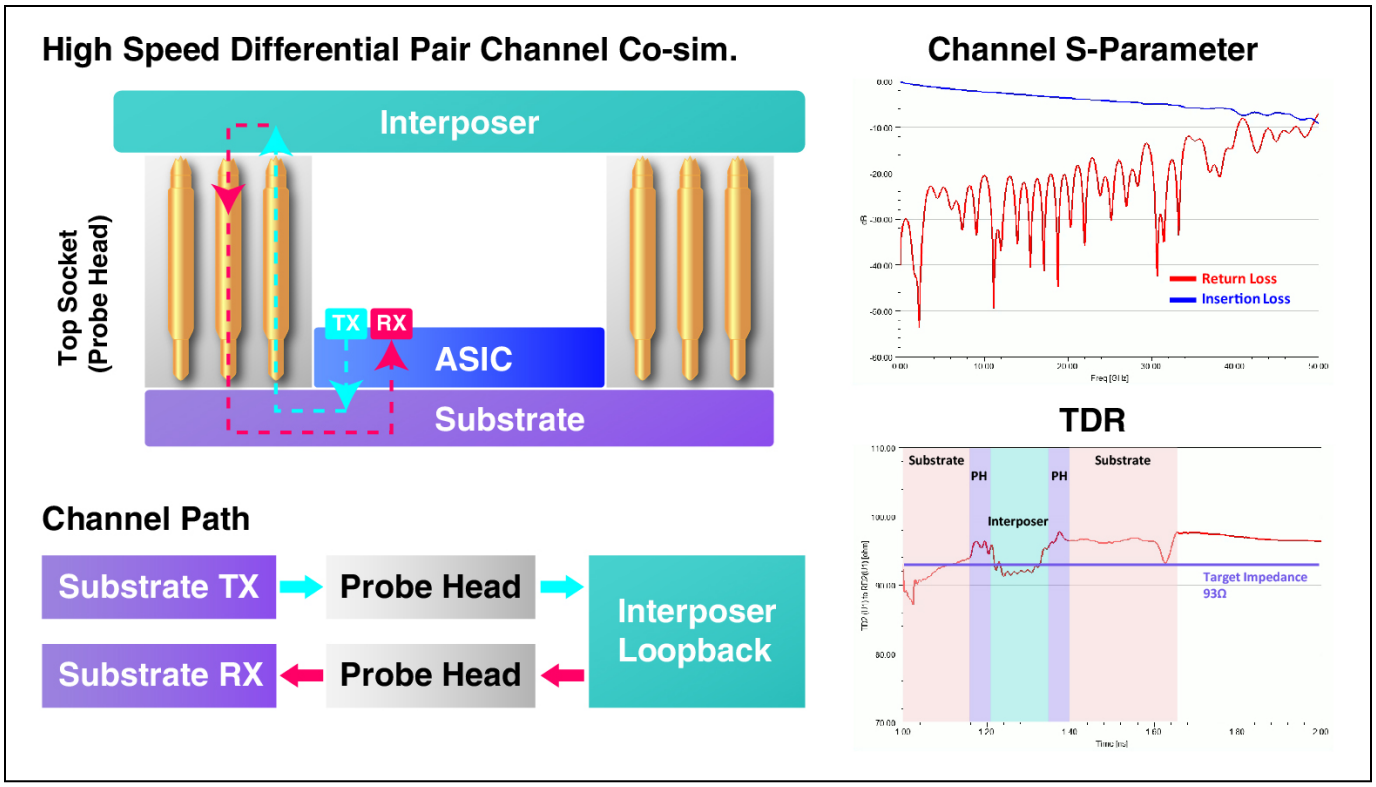

Figure 6: 112Gbps PAM4 signal loopback design in a 150µm-probe head.

of which show good correlation of insertion loss between simulation and measurement up to 85GHz (**Figure 7**). The simulation boundary condition is also proven to be a reasonable setting for such a high bandwidth.

To align with customers' thermal test requirements, we designed the water heatsink channel and performed thermal simulation, from which we obtained the expected results. After achieving satisfactory thermal performance, a prototype thermal head was manufactured to conduct the lab test and compare the difference between the simulation and actual measurement (**Figure 8**), which is a procedure similar to electrical verification and that internally proves the capability of our product. Another checkpoint of thermal simulation is to achieve thermal distribution, which will affect the fine-pitch probing stability. Distinct material selection and structural design lead to dramatic differences in thermal expansion.

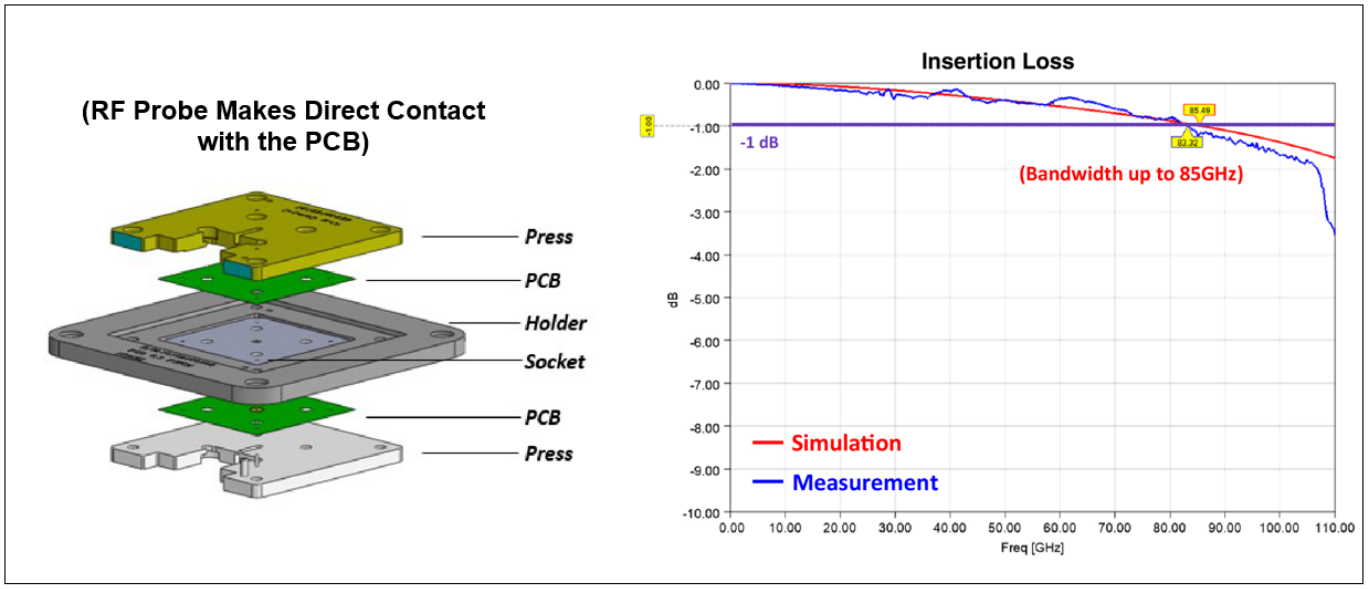

Figure 7: Electrical correlation of test fixture by 110GHz PNA .

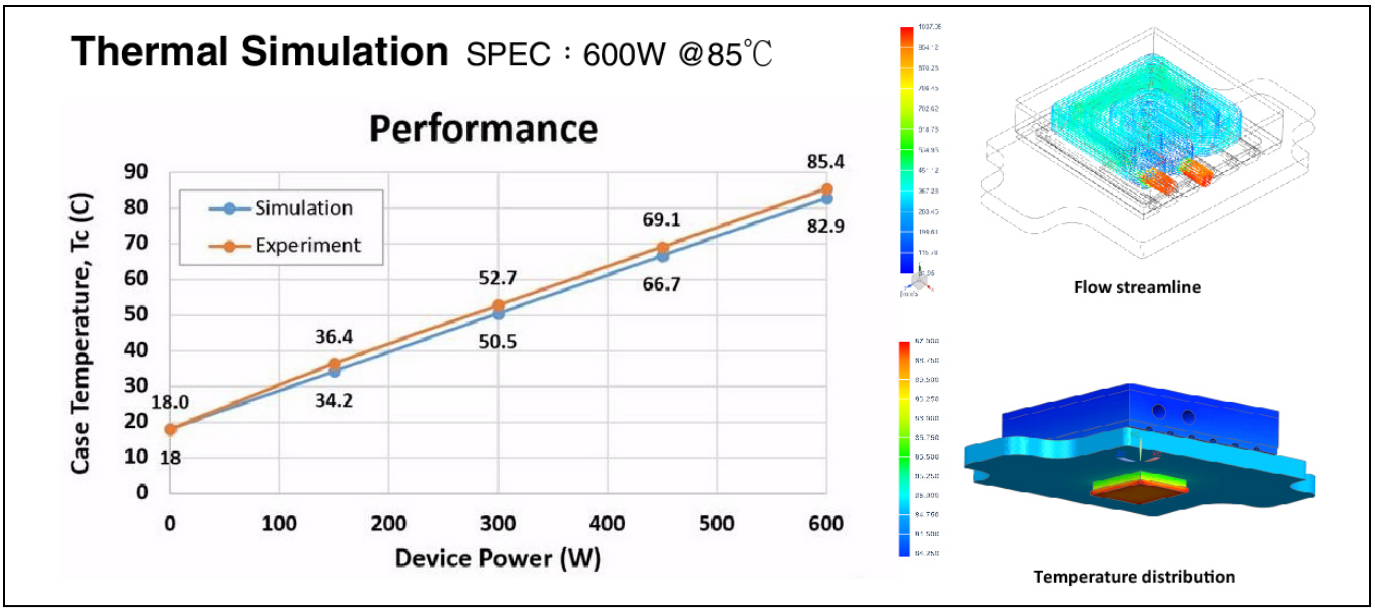

Figure 8: Thermal performance verification of HEATCon Ultra.

Summary

A double-sided probing system for 150µm-pitch CPO comprehensively integrates multiple fields, including automation for high-precision optical alignment, a 112Gbps design for a fine-pitch probe head, and a high-performance stacked thermal chuck with a double-sided probe head. Customers have used this double-sided probing system to test actual devices and the devices passed both room-temperature and high-temperature requirements. These results also support the feasibility of this test solution for the most advanced 2.5D and 3D packaged devices.

Reference

1. V. Martin, M. Pars, E. Mounier, "Co-packaged optics," https://www.yolegroup.com/product/report/co-packaged-optics-2022---focus-data-centers/#

Biography

Collins Sun is a R&D director at WinWay Technology, Taiwan. He has responsibilities in various technical fields, such as material science, high-speed product development, and thermal solutions. He received a PhD in Physics from National Sun Yat-Sen U., Taiwan. Email: collins.sun@winwayglobal.com